Features

- **Interfaces Directly to Instrument Hardware**
  - **Keyboard Velocity Scanner (up to 264 keys, 64 μs Time Accuracy, Log Time Scale)**
  - **Switches Scanner (up to 176 switches)**
  - **LED Display Controller (up to 88 LEDs)**
  - **Sliders Scanner (Built-in ADC, up to 16 Sliders)**
  - **LCD Display (8-bit Interface)**
- **Crisp Musical Response**
  - **49 MHz Built-in 16-bit Microcontroller**
  - **Interface with Keyboard/Switches through Built-in Shared Memory**
- **High Quality Sound**
  - **64-slot Digital Sound Synthesizer/Processor**
  - **Multi-algorithm: PCM with Dynamic LP Filter, FM, Delay Lines for Effects, Equalizer, Surround, Digital Audio-in Processing, etc.**
  - **Compatible with ATSAM97XX Sounds and Firmware.**
  - **48 kHz Sampling Rate**
  - **Up to 32 Mega x 16 ROM/RAM for FIrmware, Orchestrations and PCM Data**
  - **Up to 4 Channels Audio-out, 2 Channels Audio-in**
- **Top Technology**
  - **128-lead LQFP Space-saving Package**
  - **Single 12.2880 MHz Crystal Operation, Built-in PII Minimizes RFI**
- **Available Soundbanks for GM or High Quality Piano**
  - **CleanWave 1-Mbyte and 4-Mbyte Sample Sets (Free License)**
  - **High Quality Piano & Strings 2-Mbyte Sample Set**
  - **Other Sample Sets Available Under Special Licensing Conditions**
- **Quick Time to Market**
  - **Enhanced P16 Processor with C Compiler**
  - **Proven Reliable Synthesis Drivers**
  - **In-circuit Emulation with SamVS-C Debugger for Easy Prototype Development**
  - **Built-in External Flash Programming Algorithm, Allows Onboard Flash Programming.**
  - **All Existing ATSAM97xx and ATSAMA2xxx Tools Available for Sound and Soundbank Development**

Sound Synthesis

ATSAM2553 Integrated Digital Musical Instrument

1. Description

The ATSAM2553 integrates into a single chip a SAM core (64-slots DSP + 16-bit processor), a 32K x 16 RAM, an LCD display interface and a scanner allowing direct connection to velocity sensitive keyboards, switches, LEDs and sliders. With addition of a single external ROM or Flash and a stereo DAC, a complete low cost musical instrument can be built, including reverb and chorus effects, parametric equalizer, surround effects, orchestrations, pitch bend, wheel controller, without compromising on sound quality. The ATSAM2553 is housed in a standard 128-lead LQFP package.
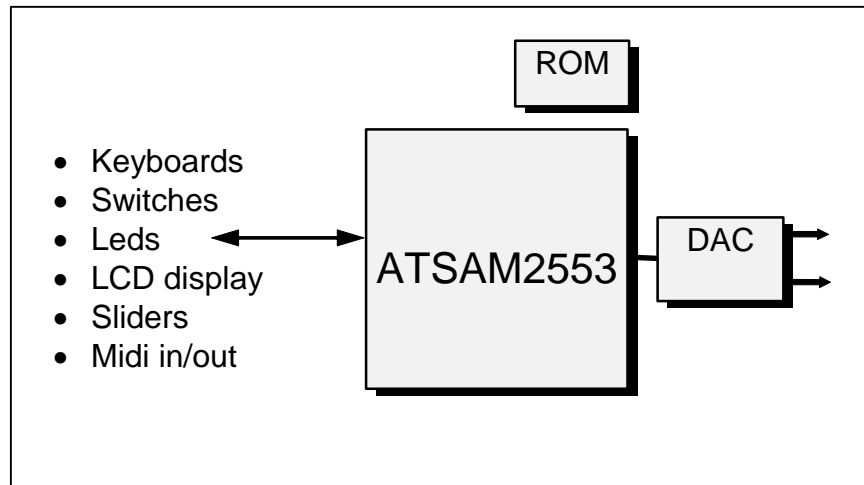
Figure 1-1. Typical Application

2. Main Features

The ATSAM2553 provides a new generation of integrated solutions for electronic musical instruments. The ATSAM2553 includes all key circuitry into a single silicon chip: sound synthesizer/processor, 16-bit control processor, interface with keyboards, switches, sliders, LEDs, LCD display, etc.

The synthesis/sound processing core of the ATSAM2553 is taken from the SAM97xx series, whose quality has already been demonstrated through dozens of different musical products: E.Pianos, home keyboards, professional keyboards, classical organs, sound expanders. The maximum polyphony is 64 voices without effects. A typical application will be 38-voice polyphony with reverb, chorus, 4-band equalizer and surround.

The ATSAM2553 is directly compatible with most available musical keyboards. This includes configuration options for spring or rubber type contacts, common anode or common cathode type matrix. A 64 µs timing accuracy for velocity detection provides a very reliable dynamic response even with low cost unweighted keyboards. The time between contacts is coded with 256 steps on a logarithmic time scale, then converted by software to a 128-step MIDI scale according to the type of keyboard and a selected keyboard sensitivity.

The ATSAM2553 can handle directly up to 176 switches. Switches, organized in matrix form, require only a serial diode. Up to 88 LEDs can be directly controlled by the ATSAM2553 in a time multiplexed way. Additional LEDs can be connected through additional external shift registers using the GPIO lines (general purpose I/O) of the ATSAM2553. The built-in analog to digital converter of the ATSAM2553 allows connecting continuous controllers like pitch-bend wheel, modulation, volume sliders, tempo sliders, etc. Up to 16 sliders can be connected.

The ATSAM2553 can be directly connected to most LCD displays through an 8-bit dedicated data bus and 3 control signals.

Configuration options allow the ATSAM2553 to cover a wide range of musical products, from the lowest cost keyboard to the high range digital piano, thanks to flexible memory and I/O organization: built-in 64K bytes RAM, up to 64M bytes external memory for firmware, orchestrations and PCM data. The external memory can be ROM, RAM or FLASH. Memory types can be mixed, but for most applications there is no need for external RAM memory as the built-in 64K bytes

RAM is enough to handle firmware variables and reverb delay lines. External flash memory can be programmed on-board from a host processor through the ATSAM2553.

The ATSAM2553 operates from a single 12.2880 MHz crystal. A built-in PLL raises the frequency to 49.152 MHz for internal processing. This allows to minimize radio frequency interference (RFI), making it easier to comply with FCC, CSA, CE standards.

A power-down feature is also included which can be controlled externally ($\overline{\text{PDWN}}$ pin). This makes the ATSAM2553 very suitable for battery operated instruments.

The ATSAM2553 has been designed with final instrument quick time to market in mind. The ATSAM2553 product development program includes key features to minimize product development efforts:

- C compiler for built-in P16 processor
- Specialized debug interface, allowing on-target software development with a source code debugger.
- Standard sound generation/processing firmware
- Standard orchestration firmware
- Windows tools for sounds, soundbanks and orchestrations developments
- Standard soundbanks
- Strong technical support available directly from Dream®

3. ATSAM2553 Internal Architecture

Figure 3-1. Internal Architecture
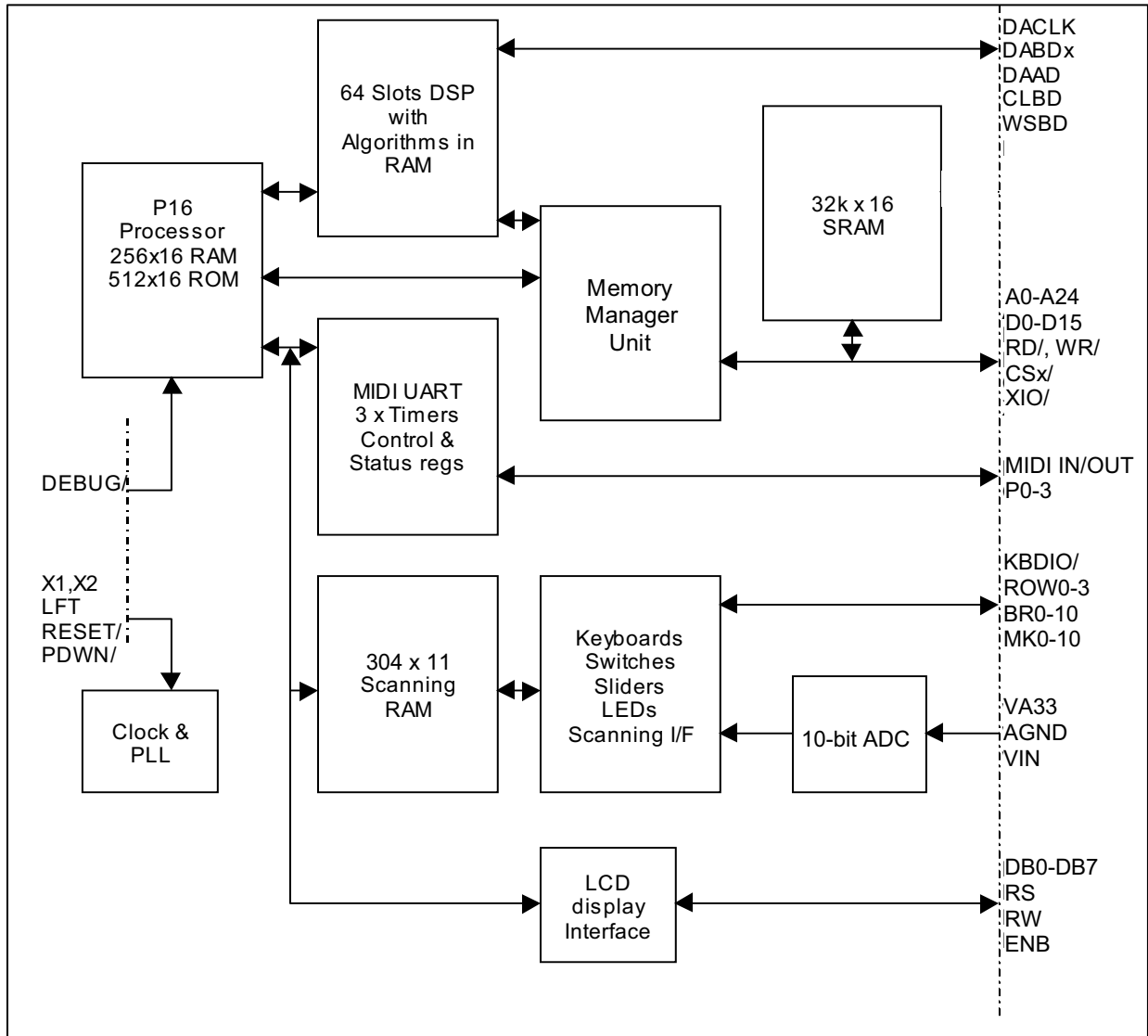
The highly integrated architecture of the ATSAM2553 combines a specialized high-performance RISC-based digital signal processor (DSP) and a general purpose 16-bit CISC-based control processor (P16). An on-chip memory management unit (MMU) allows the DSP and the control processor to share an internal 32K x 16 RAM as well as external ROM and/or RAM memory devices. An intelligent peripheral I/O interface function handles other I/O interfaces, such as the on-chip MIDI UART and 3 timers, with minimum intervention from the control processor. A keyboard/switches/sliders/LEDs autonomous scanning interface handles the specific music instrument peripherals, including accurate keyboard velocity detection and communicates with the control processor through a dedicated 304x11 dual port RAM. An LCD display interface allows direct connection to common LCD displays

3.1   DSP Engine

The DSP engine operates on a frame-timing basis with the frame subdivided into 64 process slots. Each process is itself divided into 16 micro-instructions known as "algorithm". Up to 32 DSP algorithms can be stored on-chip in the Alg RAM memory, allowing the device to be programmed for a number of audio signal generation/processing applications.

The DSP engine is capable of generating 64 simultaneous voices using algorithms such as wavetable synthesis with interpolation, alternate loop and 24dB resonant filtering for each voice. Slots may be linked together (ML RAM) to allow implementation of more complex synthesis algorithms.

A typical musical instrument application will use a little more than half the capacity of the DSP engine for synthesis, thus providing state of the art 38 voices synthesis polyphony. The remaining processing power may be used for typical functions like reverberation, chorus, surround effect, equalizer, etc.

Frequently accessed DSP parameter data are stored into 5 banks of on-chip RAM memory. Sample data or delay lines, which are accessed relatively infrequently, are stored in external ROM, or into the built-in 32K x 16 RAM. The combination of localized micro-program memory and localized parameter data allows micro-instructions to execute in 20.3 ns (49 MIPS). Separate busses from each of the on-chip parameter RAM memory banks allow highly parallel data movement to increase the effectiveness of each micro-instruction. With this architecture, a single micro-instruction can accomplish up to 6 simultaneous operations (add, multiply, load, store, etc.), providing a potential throughput of 294 million operations per second (MOPS).

3.2   Enhanced P16 Control Processor and I/O Functions

The Enhanced P16 control processor is the new version of the P16 processor with added instructions allowing C compiling. The P16 is a general-purpose 16-bit CISC processor core which runs from external memory. A debug ROM is included on-chip for easy development of firmware directly on the target system. This ROM also contains the necessary code to directly program externally connected flash memory. The P16 includes 256 words of local RAM data memory for use as registers, scratchpad data and stack.

The P16 control processor writes to the parameter RAM blocks within the DSP core in order to control the synthesis process. In a typical application, the P16 control processor parses and interprets incoming commands from the MIDI UART or from the scanning interface and then controls the DSP by writing into the parameter RAM banks in the DSP core. Slowly changing synthesis functions, such as LFOs, are implemented in the P16 control processor by periodically updating the DSP parameter RAM variables.

The P16 control processor interfaces with other peripheral devices, such as the system control and status registers, the on-chip MIDI UART, the on-chip timers and the scanning interface through specialized "intelligent" peripheral I/O logic. This I/O logic automates many of the system I/O transfers to minimize the amount of overhead processing required from the P16.

3.3   Memory Management Unit (MMU)

The Memory Management Unit (MMU) block allows external ROM and/or RAM memory resources to be shared between the synthesis/DSP and the P16 control processor. This allows a single ROM device to serve as sample memory storage for the DSP and as program storage for the P16 control processor. An internal 32K x 16 RAM is also connected to the MMU, allowing RAM resources to be shared between the DSP for delay lines and the P16 for program data.

3.4 Keyboards/Switches/Sliders/LEDs Scanning Interface

The scanning interface consists of hardwired logic. It time multiplexes keyboard, switches and LEDs connections therefore minimizing the amount of wiring required. It communicates with the P16 through an 304 x 11 dual port RAM and a few control registers. When a new incoming event is detected, such as key-on, key-off or switch change, the scanning interface will notify the P16 by indicating the type of event. The P16 then simply reads the dual port RAM to get the corresponding parameter, such as velocity or switch status. Conversely, the P16 simply writes into the dual port RAM the led states to be displayed and the scanning interface will then take care of time multiplexing the display.

The scanning interface uses an unique key velocity detect scheme with a pseudo-logarithmic time scale. This allows velocities to be accurately detected, even when keyboard keys are pressed very softly.

Finally a built-in 10-bit analog to digital converter (ADC) allows the connection of up to 16 continuous controllers through external analog multiplexers such as the 4051.

3.5 LCD Display Interface

The LCD display interface uses a dedicated bidirectional data bus (DB0-DB7) an Instruction/data control RS, a read write signal R/W and an enable signal ENB. Built-in features are included to accommodate even the slowest LCD displays.

3.6 Flash Programming

The ATSAM2553 enables programming Flash memories in three different ways:

- Blank Flash programming is done by the debug interface. This mode is very slow and should be reserved for the initial boot sector programming.

- Program update. All the Flash content can be re-programmed. The ATSAM2553 cannot play music during the Flash erase and programming. A specific firmware is used to program Flash with the DSP

- Parameters update, e.g. in keyboard applications, backup parameter and sequencer song. If the Flash enables concurrent read during program/erase, it is possible to backup parameters in the upper memory plane while the µp firmware is running on the lower plane. The ATSAM2553 cannot play music during the parameter backup because sound samples are stored in both memory planes.

3.7 Flash Features

- 3.3v or 5v

- Access time: 90 ns (for 12.288 MHz crystal)

- Dual plane with concurrent read while program/erase recommended for parameters backup.

4. Pin Description

5VT indicates a 5 volt tolerant Input or I/O pin.

4.1 Pins by Function

Table 4-1. Power Supply

Pin Name	Pin#	Type	Function
GND	1, 14, 33, 48, 65, 85, 97, 98, 116	PWR	DIGITAL GROUND All pins should be connected to a ground plane
AGND	16	PWR	ANALOG GROUND for the ADC. Should be connected to a clean analog ground.
VD33	18, 32, 40, 49, 64, 84, 96, 115, 128	PWR	POWER SUPPLY, 3.3V ± 10% All pins should be connected to a VD33 plane
VD18	100	PWR	Power for the internal PLL, +1.8V nominal (1.8V ± 10%). These pins can be connected to the output of the regulator OUTVC18 (pin 41). A 100 nF decoupling capacitor should be connected between this pin and PLL ground (pin98)
VA33	17	PWR	Analog power for the ADC, +3.3V nominal (3,3V ± 10%).

Power supply decoupling note: like all high speed HCMOS ICs, proper decoupling is mandatory for reliable operation and RFI reduction. The recommended decoupling is 100 nF at each corner of the IC with an additional 10 µFT bulk capacitor close to the X1, X2 pins.

Table 4-2. Serial MIDI

Pin Name	Pin#	Type	Function
MIDI-IN	127	IN 5VT	Serial MIDI IN. This pin has a built-in pull up
MIDI-OUT	126	OUT	Serial MIDI OUT.

Table 4-3. External PCM ROM/RAM/IO

Pin Name	Pin#	Type	Function
WA0-WA24	42-47,50-55,66-78	OUT	External memory I/O Address, up to 32 Mega x 16 for direct ROM/RAM connection.
WD0-WD15	21-31,34-38	I/O 5VT	External memory I/O data. Data is read (input) when $\overline{RD}$ is low, written (output) when $\overline{WR}$ is low.
$\overline{WOE}$	94	OUT	External ROM/RAM peripherals output enable.
$\overline{WWE}$	95	OUT	External RAM peripherals write enable.
$\overline{WCS0}$ -$\overline{WCS1}$	92,93	OUT	Programmable chip selects. Can be configured to handle several ROMs or mixed RAM/ROM/Flash.
$\overline{XIO}$	20	OUT	External peripheral chip select. $\overline{XIO}$ maps its peripheral into 4k bytes address space for optional further decoding.

Table 4-4.   Keyboard, Switches, LEDs, Sliders, Scanning

Pin Name	Pin#	Type	Function
$\overline{\text{KBDIO}}$	19	OUT	If 1 BR[0-10] & MK[0-10] hold keyboard contact input data. If 0 BR[0-10] holds switch status input, MK[0-10] holds led data output.
ROW0-ROW3	56-59	OUT	Row select: keyboard, switches/LEDs, external slider analog multiplexer (4051) channel select. Sixteen rows combined with eleven BR/MK columns allow to control 176 keys, 176 switches, 88 leds and 16 sliders. The programmable bit P0 can be programmed to be used as ROW4. This allows to use keyboards with matrix other than 8*11 (e.g. 22*4) or multiple keyboards up to 264 keys.
BR0-BR10	104-114	IN 5VT	Kbd contact 1/switch status. When $\overline{\text{KBDIO}}$ =1 then BR[0-10] holds the keyboard key-off or first contact status. This can be configured as normally close (spring type), normally open (rubber type), common anode or common cathode contact diodes. When $\overline{\text{KBDIO}}$ = 0 then BR[0-10] holds the switch status from ROW[0-4].
MK0-MK10	79-83,86-91	I/O 5VT	Kbd contact 2/LED data. When $\overline{\text{KBDIO}}$ = 1 then MK[0-10] holds the keyboard key-on or second contact status. This can be configured as common anode or common cathode contact diodes. When $\overline{\text{KBDIO}}$ = 0 then MK[0-10] holds the LED data from ROW[0-4]
VIN	15	ANA	Slider analog input. Ranges from AGND to VA33. Should hold the ROW[0-3] slider voltage. Multiple sliders should be connected through external analog multiplexer(s) like 4051.

The following signals are controlled by firmware, therefore their timing relationships is determined by firmware only.

Table 4-5.   LCD Display Interface

Pin Name	Pin#	Type	Function
RS	5	OUT	Select Instruction (LOW) or Data (HIGH)
RW	4	OUT	Select Write (LOW) or Read (HIGH)
ENB	3	OUT	Enable, active high
DB0-DB7	6-13	I/O 5VT	Bi-directional data bus

The ATSAM2553 connects to a variety of stereo DACs or CODECs from 16 to 20 bits, with Japanese or I2S format. When Japanese format is used, only 16 bits are supported without external circuitry

Table 4-6. Digital Audio Group

Pin Name	Pin#	Type	Function
CKOUT	120	OUT	Master clock for Σ/Δ DAC (256 x Fs)
DABD0-DABD1	123,124	OUT	Serial data for 2 stereo output channels.
DAAD	125	IN 5VT	Serial data for 1 stereo input channel
CLBD	121	OUT	Digital audio bit clock
WSBD	122	OUT	Digital audio left/right select

Table 4-7. Miscellaneous Group

Pin Name	Pin#	Type	Function
P0-P3	60-63	I/O 5VT	General purpose programmable I/O pins. P0 pin can be used as general purpose I/O or as ROW4 function. These pins have a built-in pull down.
DBCLK	117	IN 5VT	Debug clock, should be connected to VD33 under normal operation. If DBCLK is found low just after RESET, then the internal ROM debugger/Flash programmer is started.
DBDATA	119	I/O 5VT	Debug data, allows serial communication for debug/Flash programming. This pin has a built-in pull down.
DBACK	118	OUT	Debug ack, toggled each time a bit is received/sent on DBDATA.
$\overline{\text{RESET}}$	103	IN 5VT	Reset input, active low. This is a Schmitt trigger input, allowing direct connection of a RC network.
$\overline{\text{PDWN}}$	39	IN	Power down, active low. When power down is active, $\overline{\text{WCS0}}$, $\overline{\text{WCS1}}$, $\overline{\text{XIO}}$, $\overline{\text{WWE}}$, $\overline{\text{WOE}}$ address and data lines are floated. All other outputs are set to 0. The crystal oscillator is stopped, OUTVC18 is set to 0 and 1.8V supply voltage is removed from the core. To exit from power down, $\overline{\text{PDWN}}$ must be set to VD33, then $\overline{\text{RESET}}$ applied. When unused this pin must be connected to VD33.
OUTVC18	41	PWR	3.3V to 1.8 V regulator output. The built-in regulator gives 1.8V for internal use (core supply). PLL supply pin VD18 could also be connected to this pin. Decoupling capacitors 470 pF in parallel with 2.2 or 4.7 µF must be connected between OUTVC18 and GND.
X1-X2	101,102	-	12.288 MHz (nominal) crystal connection. An external clock can also be used at X1.
TEST0-TEST1	2,99	IN	Test pins, should be grounded.

4.2   Pinout by Pin Number 128-lead LQFP Package

Table 4-8.   Pinout by Pin#

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	**GND**	33	**GND**	65	**GND**	97	**GND**
2	TEST0	34	WD11	66	WA12	98	**GND**
3	ENB	35	WD12	67	WA13	99	TEST1
4	RW	36	WD13	68	WA14	100	**VD18**
5	RS	37	WD14	69	WA15	101	X1
6	DB0	38	WD15	70	WA16	102	X2
7	DB1	39	$\overline{\text{PDWN}}$	71	WA17	103	$\overline{\text{RESET}}$
8	DB2	40	**VD33**	72	WA18	104	BR0
9	DB3	41	OUTVC18	73	WA19	105	BR1
10	DB4	42	WA0	74	WA20	106	BR2
11	DB5	43	WA1	75	WA21	107	BR3
12	DB6	44	WA2	76	WA22	108	BR4
13	DB7	45	WA3	77	WA23	109	BR5
14	**GND**	46	WA4	78	WA24	110	BR6
15	VIN	47	WA5	79	MK0	111	BR7
16	**AGND**	48	**GND**	80	MK1	112	BR8
17	**VA33**	49	**VD33**	81	MK2	113	BR9
18	**VD33**	50	WA6	82	MK3	114	BR10
19	$\overline{\text{KBDIO}}$	51	WA7	83	MK4	115	**VD33**
20	$\overline{\text{XIO}}$	52	WA8	84	**VD33**	116	**GND**
21	WD0	53	WA9	85	**GND**	117	DBCLK
22	WD1	54	WA10	86	MK5	118	DBACK
23	WD2	55	WA11	87	MK6	119	DBDATA
24	WD3	56	ROW0	88	MK7	120	CKOUT
25	WD4	57	ROW1	89	MK8	121	CLBD
26	WD5	58	ROW2	90	MK9	122	WSBD
27	WD6	59	ROW3	91	MK10	123	DABD0
28	WD7	60	P0	92	$\overline{\text{WCS0}}$	124	DABD1
29	WD8	61	P1	93	$\overline{\text{WCS1}}$	125	DAAD
30	WD9	62	P2	94	$\overline{\text{WOE}}$	126	MIDI_OUT
31	WD10	63	P3	95	$\overline{\text{WWE}}$	127	MIDI_IN
32	**VD33**	64	**VD33**	96	**VD33**	128	**VD33**

5.   Marking

Figure 5-1.   ATSAM2553 Marking

dream
FRANCE

SAM2553
YYWW 58A66C
XXXXXXXXX

PIN 1

6. Mechanical Dimensions 128-lead LQFP Package

Figure 6-1. Mechanical Dimensions
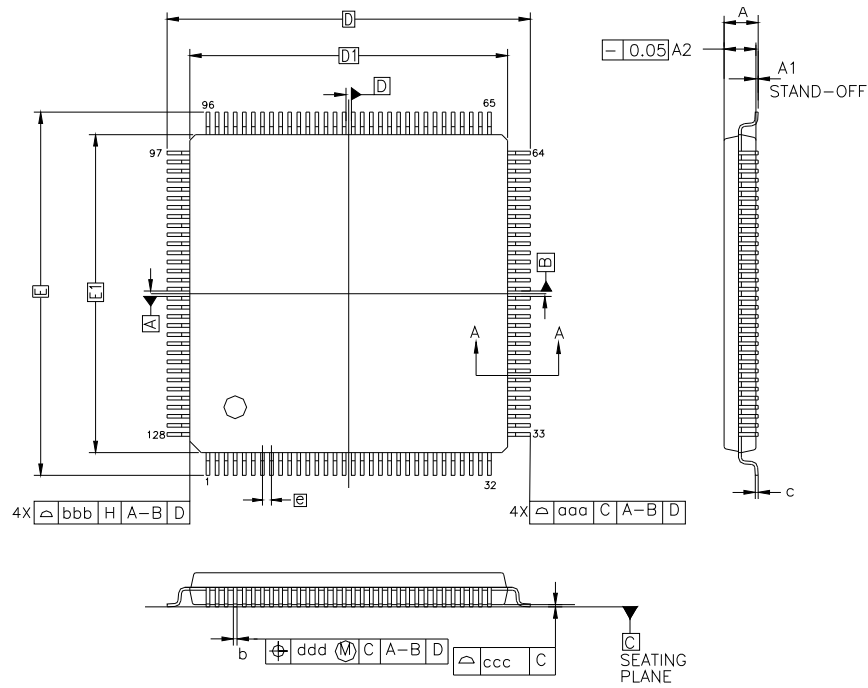
ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A 1	0.05	—	0.15	0.002	—	0.006
A 2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BASIC			0.630 BASIC		
D 1	14.00 BASIC			0.552 BASIC		
E	16.00 BASIC			0.630 BASIC		
E 1	14.00 BASIC			0.552 BASIC		
R 2	0.08	—	0.20	0.003	—	0.008
R 1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ 1	0°	—	—	0°	—	—
θ 2	11°	12°	13°	11°	12°	13°
θ 3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	0.127	0.16	0.004	0.005	0.006
L1	1.00 REF			0.039 REF		
L	0.45	0.60	0.75	0.018	0.024	0.030
S	0.20	—	—	0.008	—	—
b	0.13	—	0.23	0.005	—	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
e	0.40 BSC.			0.016 BSC.		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

7. Electrical Characteristics

7.1 Absolute Maximum Ratings(*)

All voltages with respect to 0V, GND = 0V.

Temperature under bias.................................. -55°C to +125°C
Storage Temperature .... -65°C to +150°C
Voltage on any 5 volt tolerant pin .... -0.3 to 5.5V
Voltage on any non 5 volt tolerant pin .... -0.3 to V_{D33} + 0.3V
Supply Voltage..
V_{D33}..-0.3V to 3.6V
V_{D18}..-0.3V to 2V
V_{A33}..-0.3V to 3.6V
Maximum IOL per I/O pin... 10 mA
Maximum IOH per I/O pin .... 10 mA
Maximum Output current from OUTVC18 pin (max duration = 1sec) IREGO .... 70 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

Table 7-1. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{D33}	Supply voltage	3	3.3	3.6	V
V_{D18}	Supply voltage (PLL)	1.65	1.8	1.95	V
V_{A33}	Supply voltage (PLL)	3	3.3	3.6	V
IREGO	OUTVC18 output current	-	30		mA
T_A	Operating ambient temperature	-25	-	70	°C

7.3 DC Characteristics

Table 7-2. DC Characteristics (T_A = 25°C, V_{D33} = 3.3V ± 10%, V_{D18} = 1.8V ± 10%)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	-0.3	-	0.8	V
V_{IH}	High level input voltage on non-5VT pins	2	-	3.6	V
V_{IH}	High level input voltage on 5VT pins	2	-	5.5	V
V_{OL}	Low level output voltage IOL=4mA	-	-	0.4	V
V_{OH}	High level output voltage IOH=4mA	VD33-0.4	-	-	V
ID18	Power supply current at (crystal freq.=12.288 MHz)		0.7		mA
ID33			36		mA
–	Power down supply current		0.6		mA
Rud	Pull-up or Pull-down resistor	8	13	25	kOhm

8. Timings

All timings conditions: VD33=3.3V, VD18=1.8V, TA=25°C, all outputs except X2, have load capacitance = 30 pF.

All timings refer to tck, which is the internal master clock period.

The internal master clock frequency is 4 times the frequency at pin X1. Therefore tck=txtal/4.

The sampling rate is given by 1/(tck*1024). The maximum crystal frequency/clock frequency at X1 is 12.288 MHz (48 KHz sampling rate).

8.1 Crystal Frequency Selection Considerations

There is a trade-off between the crystal frequency and the support of widely available external ROM/Flash components. Table 8-1 allows to select the best fit for a given application;

Table 8-1. Crystal Frequency Selection Chart

Sample Rate (kHz)	Xtal (MHz)	tck (ns)	ROM tA (ns)	Comments
48	12.288	20.35	92	Recommended for current designs.
44.1	11.2896	22.14	101	
37.5	9.60	26.04	120	
31.25	8.00	31.25	146	

Using 12.288 MHz crystal frequency allows to use widely available ROM/Flash with 90 ns access time, while providing state of the art 48 kHz sampling rate.

8.2 Scanning (Keyboard, Switches, LEDs, Sliders

Figure 8-1. Scanning (Keyboard, Switches, LEDs, Sliders
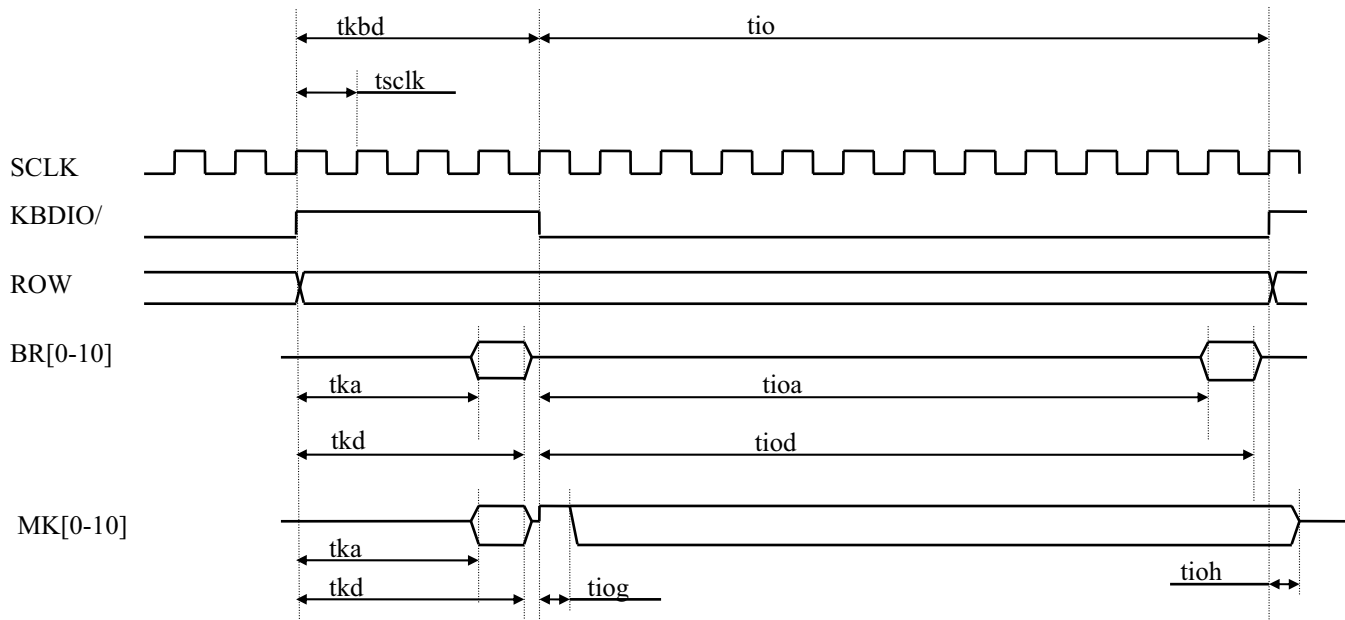
All timings relative to 12.288 MHz crystal between X1 and X2.

Table 8-2. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
Tkbd	Keyboard access ($\overline{\text{KBDIO}}$ high time)		1.3		µs
Tio	Switches/leds access ($\overline{\text{KBDIO}}$ low time)		3.9		µs
Tsclk	Internal scanning clock period		325		ns
Tka	Keyboard valid from rising $\overline{\text{KBDIO}}$			1.1	µs
tkd	Break (contact1) and make (contact2) data from Keyboard floating from rising $\overline{\text{KBDIO}}$	1.2		1.5	µs
tioa	Switch data valid from falling $\overline{\text{KBDIO}}$			3.6	µs
tiod	Switch data floating from falling $\overline{\text{KBDIO}}$	3.7		4	µs
tiog	LED data MK guard time	27		163	ns
tioh	LED data floating from rising $\overline{\text{KBDIO}}$	0		82	ns

8.3   External ROM/Flash, RAM, I/O Read Timing

Figure 8-2.   External ROM/Flash, RAM, I/O Read Timing
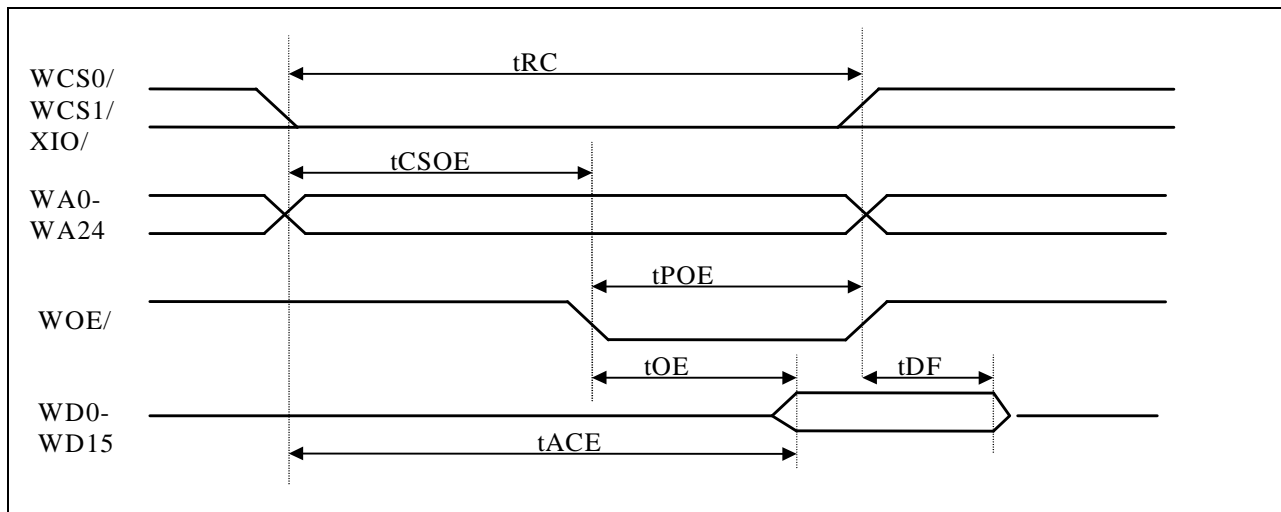
Table 8-3.   Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
tRC	Read cycle time	5*tck	-	6*tck	ns
tCSOE	Chip select low / address valid to WOE/ low	2*tck-5	-	3*tck+5	ns
tPOE	Output enable pulse width	-	3*tck	-	ns
tACE	Chip select/address access time	5*tck-5	-	-	ns
tOE	Output enable access time	3*tck-5	-	-	ns
tDF	Chip select or WOE/ high to input data Hi-Z	0	-	2*tck-5	ns

8.4 External Flash, RAM, I/O Write Timing

Figure 8-3. External Flash, RAM, I/O Write Timing
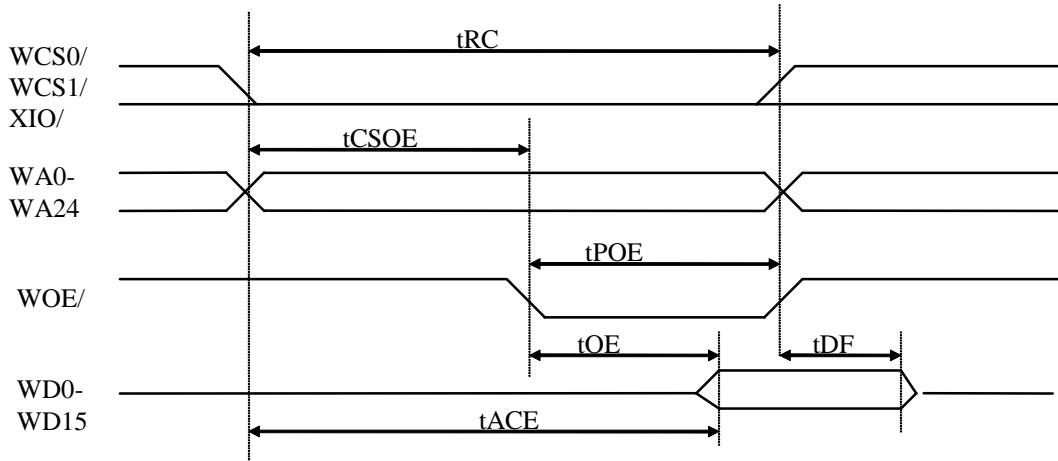
Table 8-4. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
tWC	Write cycle time	5*tck	-	6*tck	ns
tCSWE	Write enable low from CS/ or Address or WOE/	2*tck-10	-	-	ns
tWP	Write pulse width	-	4*tck	-	ns
tDW	Data out setup time	4*tck-10	-	-	ns
tDH	Data out hold time	10	-	-	ns

8.5 Digital Audio

Figure 8-4. Digital Audio
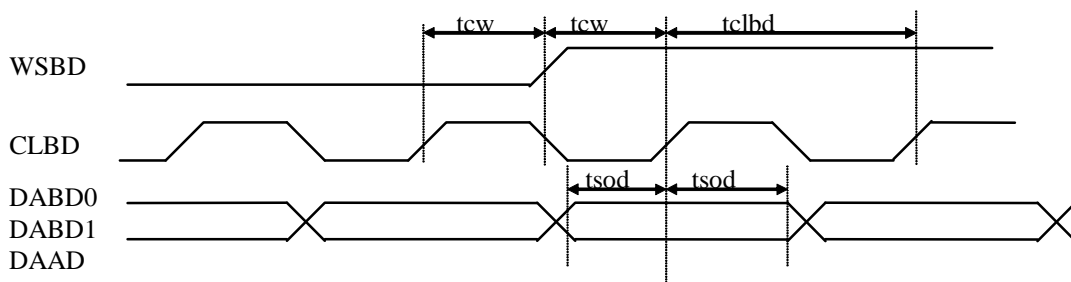
Table 8-5. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
tcw	CLBD rising to WSBD change	8*tck-10	-	-	ns
tsod	DABD valid prior/after CLBD rising	8*tck-10	-	-	ns
tclbd	CLBD cycle time	-	16*tck	-	ns

Figure 8-5. Digital Audio Frame Format
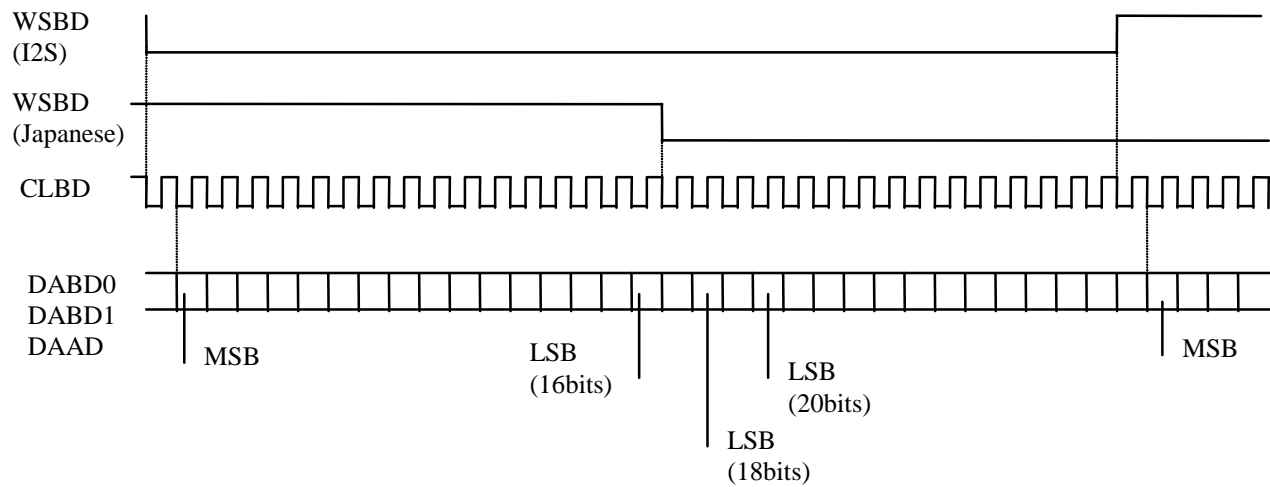
9. Recommended Crystal Compensation

Figure 9-1. Recommend Crystal Compensation
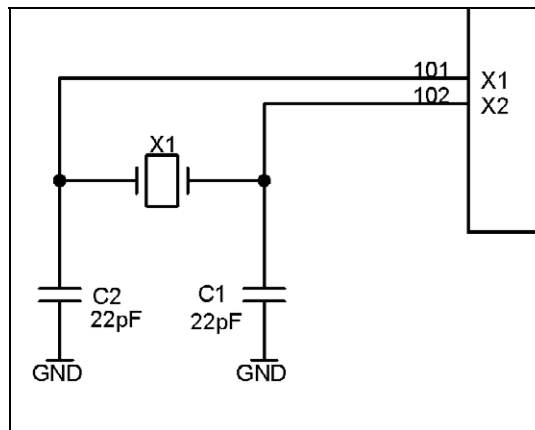
10. Recommended Board Layout

Like all HCMOS high integration ICs, following simple rules of board layout is mandatory for reliable operations:

• GND, VD33, VD18 distribution, decouplings

All GND, AGND, VD33, VD18, VA33 pins should be connected. A GND plane is strongly recommended below the ATSAM2553. The board GND + VD33 planes could be in grid form to minimize EMI.

Recommended VD18 decoupling is 0.1µF, close to the VD18 pin and 470pF in parallel with 2.2 or 4.7µF, close to OUTVC18 pin. VD33 requires 0.1 µF at each corner of the IC with an additional 10 µFT capacitor that should be placed close to the crystal.

• Crystal

The paths between the crystal, the crystal compensation capacitors and the ATSAM2553 should be short and shielded. The ground return from the compensation capacitors should be the GND plane from ATSAM2553.

• Busses

Parallel layout from DB0-DB7 and WA0-WA24/WD0-WD15 should be avoided. The DB0-DB7 bus is an asynchronous type bus. Even on short distances, it can induce pulses on WA0-WA24/WD0-WD15 which can corrupt address and/or data on these busses.

A ground plane should be implemented below the DB0-DB7 bus.

A ground plane should be implemented below the WA0-WA24/WD0-WD15 bus, which connects both to the ROM/Flash grounds and to the ATSAM2553.

• Analog section

A specific AGND ground plane should be provided, which connects by a single trace to the GND ground. No digital signals should cross the AGND plane. Refer to the CODEC vendor recommended layout for correct implementation of the analog section

11. Typical Keyboard, Switches, LEDs, Sliders Connection
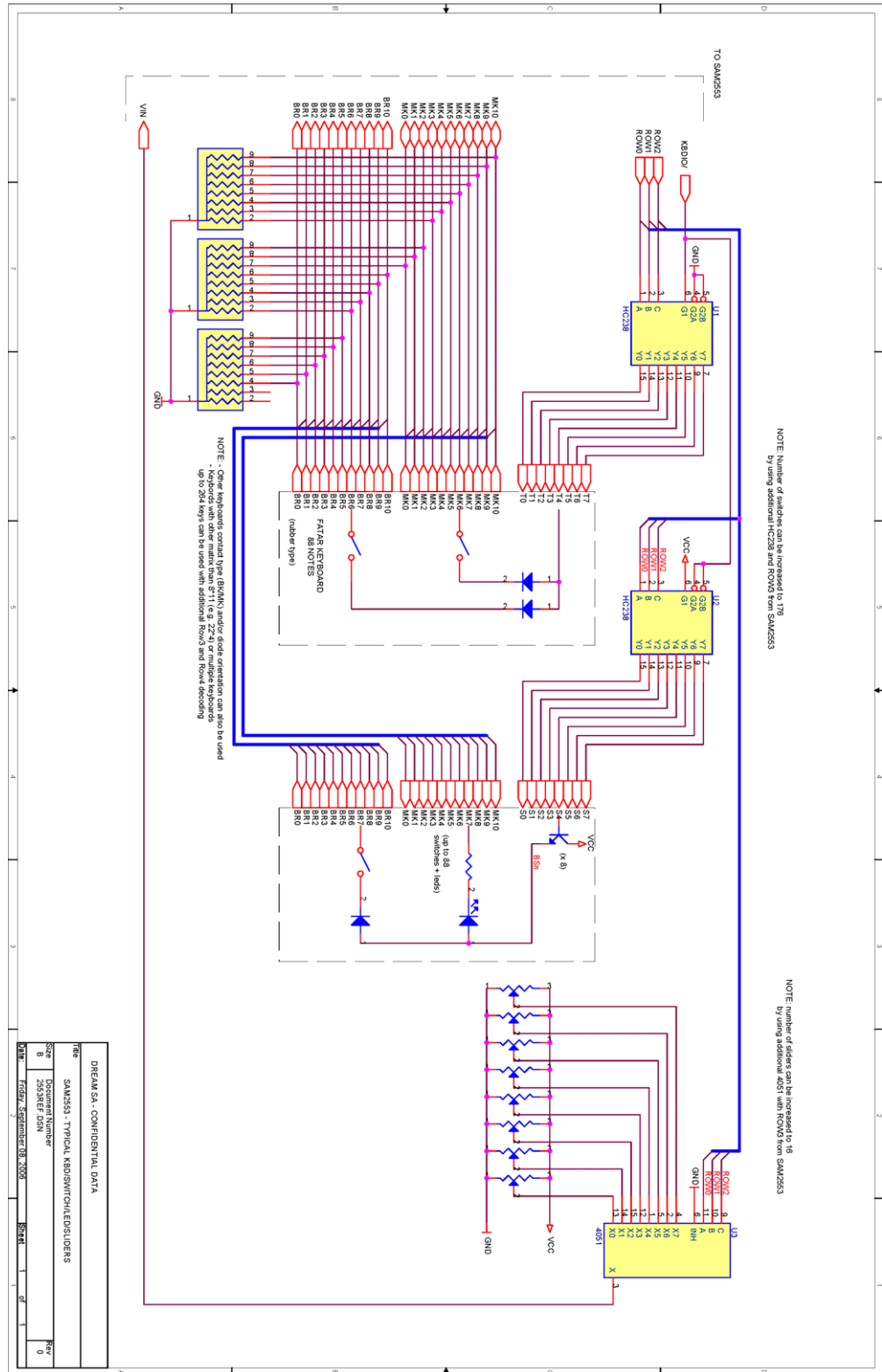
12. Overview of Operations

Note: the reader should be familiar with the ATSAM97xx series operation. Refer to the ATSAM9707 product development kit "prgdvkit.pdf" document.

This chapter describes operations and registers specific to the ATSAM2553.

12.1 Memory Mapping

Size (in word)	Address Low	Address High	Access
256	000:0000	000:00FF	ATSAM97xx standard routine ROM
768	000:0100	000:03FF	Built in debug ROM
32M - 1K	000:0400	1FF:FFFF	External ROM/Flash (WCS0/)
32K	200:0000	200:7FFF	Built in SRAM
4K	200:8000	200:8FFF	External memory page XIO (XIO/)
4K	200:9000	200:9FFF	Not used
216K	200:A000	203:FFFF	Not used
32M - 256K	204:0000	3FF:FFFF	External SRAM ($\overline{WCS1}$)

12.2 I/O Mapping

Write	Read	
0-9	0-9	Standard ATSAM97xx I/O (Refer to prgdvkit.pdf)
0A	0A	LCD port
0B	X	Keyboard config
0C - 0E	0C - 0E	Scanning port ADD0-2
0F	0F	GPIO Control/Status

12.3 LCD Interface

The ATSAM2553 can be directly connected to most LCD displays.

The ATSAM2553 provides an 8-bit data bus, DB0-DB7 and 3 output control pins RS, RW, ENB.

All the LCD pins are controlled by I/O Access ADD 0AH. The IO reads only the 8-bit data bus. The IO writes into the 11-bit LCD_Reg:

LCD_Reg[7:0]	DB[7:0]
LCD_Reg[8]	RS
LCD_Reg[9]	RW
LCD_Reg[10]	ENB

IO Access	IO Data	LCD_Reg[10]	DB[7:0]	RW	Comments
Write	IOD[10:0] (IOD[9]=0)	IOD[10:0] LCD_Reg[9]=0	IOD[7:0] output	0	Set LCD in write mode
Write	IOD[10:0] (IOD[9]=1)	IOD[10:0] LCD_Reg[9]=1	LCD_D[7:0] input	1	Set LCD in read mode
Read	xx	LCD_Reg[9]=0	LCD_Reg[7:0] output	0	Invalid read from LCD in write mode
Read	xxx, LCD_D[7:0]	LCD_Reg[9]=1	LCD_D[7:0] input	1	Read from LCD

12.4 Keyboard Configuration Register

The configuration register allows dealing with a variety of keyboards. This write only 6-bit register is mapped at the address OBH in the I/O space.

Reg[0] = contact type   0 for rubber type contact

                                    1 for spring type contact

Reg[1] = diode wiring   0 for common anode wiring

                                    1 for common cathode wiring

The default configuration (power-up) is common anode (Reg[1]=0) and rubber contact (Reg[0]=0) which corresponds to most popular keyboards.

Reg[3:2] = Scanning clock divider. (Default 00).

Reg[3:2]}	Divide Factor
00	1
01	2
10	4
11	Not Used

Reg[5:4] = Scanning matrix. (Default 00).

Reg[5:4]}	Scanning Matrix
00	Row[2:0]
01	Row[3:0]
10	Row[4:0]
11	Not Used

12.5 Scanning Interface

The ATSAM2553 has built-in specialized hardware which allows the following functions:

- Scanning of up to 264 keys from an external keyboard, with key-on and key-off velocity measurement (time between contacts)
- Scanning of up to 176 switches
- Time multiplex control of up to 88 LEDs
- Analog to digital conversion of up to 16 analog sources

The P16 interfaces with the scanning using a 3 addresses port located at 0CH to 0EH in the I/O mapping.

This port enables access to the keyboard RAM. This 304 x 11 RAM is mapped as follows:

* Key Page 0	* Key Page 1	* Key Page 2
00H Key velocity and status for MK0/BR0 at row [2:0]	00H Key velocity and status for MK0/BR0 at row [2:0]	00H Key velocity and status for MK0/BR0 at row [2:0]
08H Key velocity and status for MK1/BR1 at row [2:0]	08H Key velocity and status for MK1/BR1 at row [2:0]	08H Key velocity and status for MK1/BR1 at row [2:0]
10H Key velocity and status for MK2/BR2 at row [2:0]	10H Key velocity and status for MK2/BR2 at row [2:0]	10H Key velocity and status for MK2/BR2 at row [2:0]
18H Key velocity and status for MK3/BR3 at row [2:0]	18H Key velocity and status for MK3/BR3 at row [2:0]	18H Key velocity and status for MK3/BR3 at row [2:0]
20H Key velocity and status for MK4/BR4 at row [2:0]	20H Key velocity and status for MK4/BR4 at row [2:0]	20H Key velocity and status for MK4/BR4 at row [2:0]
28H Key velocity and status for MK5/BR5 at row [2:0]	28H Key velocity and status for MK5/BR5 at row [2:0]	28H Key velocity and status for MK5/BR5 at row [2:0]
30H Key velocity and status for MK6/BR6 at row [2:0]	30H Key velocity and status for MK6/BR6 at row [2:0]	30H Key velocity and status for MK6/BR6 at row [2:0]
38H Key velocity and status for MK7/BR7 at row [2:0]	38H Key velocity and status for MK7/BR7 at row [2:0]	38H Key velocity and status for MK7/BR7 at row [2:0]
40H Key velocity and status for MK8/BR8 at row [2:0]	40H Key velocity and status for MK8/BR8 at row [2:0]	40H Key velocity and status for MK8/BR8 at row [2:0]
48H Key velocity and status for MK9/BR9 at row [2:0]	48H Key velocity and status for MK9/BR9 at row [2:0]	48H Key velocity and status for MK9/BR9 at row [2:0]
50H Key velocity and status for MK10/BR10 at row	50H Key velocity and status for MK10/BR10 at row [2:0]	50H Key velocity and status for MK10/BR10 at row [2:0]
58H LED data	58H	58H
60H SWITCH data		
70H ADC data		
7FH		

Note: There are three possible values for Key page.

0: Value sampled at Row4 = 0, Row3 = 0

1: Value sampled at Row4 = 0, Row3 = 1

2: Value sampled at Row4 = 1, Row3 = 0

3: Not used.

12.5.1   KBD Status (I/O add OCH Read-only)

- D[7] KRQ flag = 1 indicates that a key-on or key-off has been detected and that the P16 service is requested. This flag is automatically cleared by a write to data H for the detected key.
- D[6:0] specify which keyboard key is requesting the service, valid only if KRQ flag = 1. Key nb range from 0 to 87.
- D[9:8] specify the Key page

12.5.2   RAM Add (I/O add OCH Write-only)

- D[6:0] RAM address
- D[7] don't care
- D[9:8] Key page

Key Page	Add	Index	Content
Value: 0,1,2	00H to 57H	8*i+row[2:0]	Key velocity and status
Don't-care	58H to 5FH	row[2:0]	Led data
Don't-care	60H to 6FH	row[3:0]	Switch status
Don't-care	70H to 7FH	row[3:0]	ADC value

"i" refers to the Mki or Bri signal number which ranges from 0 to 10. For example, the information regarding the key at row 2, column MK5/BR5, will be found at RAM address 8*5+2=42.

The scanning hardware cycles the row[2:0] signals from 0 to 7 to the output pins in 41.6 µs (5.2 µs per row).

12.5.3   RAM Data (I/O add ODH Read/Write)

Data[10:0]   I/O add ODH, Data[10:0]

Data[15:11]   don't care

Scanning RAM data format:

Bit–>	10	9	8	7	6	5	4	3	2	1	0
Key velocity & status	SRQ	ON	BUSY	VEL							
LED data	MK10	MK9	MK8	MK7	MK6	MK5	MK4	MK3	MK2	MK1	MK0
Switch data	BR10	BR9	BR8	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
ADC status	X	X	X	ADC DATA							

Key velocity & Status:

- SRQ: If 1, indicates that the velocity detection is completed and that this key requests attention from the P16. In this case BUSY = 0, ON and VEL hold valid information.
- ON: 1 indicates key-on, 0 indicates key-off. Valid only if SRQ = 1.
- BUSY: Used internally by the scanning hardware, indicates "velocity detection in progress".

- VEL: From 0 to 255, valid only if SRQ = 1, indicates the time between contacts. Time is depending on Scanning divider and Scanning matrix configuration.
  Time = TimeCount x $2^{\text{Scanning divider}}$ x (1 + Scanning matrix)
    - 0 < VEL < 128: TimeCount = VEL x 41.6 µs.
    - 128 < VEL < 192: TimeCount = 128 x 41.6 µs + (VEL - 128) x 2 x 41.6µs.
    - 192 < VEL < 224: TimeCount = 2 x 128 x 41.6 µs + (VEL - 192) x 4 x 41.6µs.
    - 224 < VEL < 240: TimeCount = 3 x 128 x 41.6 µs + (VEL - 224) x 8 x 41.6µs.
    - 240 < VEL < 255: TimeCount = 4 x 128 x 41.6 µs + (VEL - 240) x 16 x 41.6µs.
- LED data: The P16 should write to these locations the MK information which should appear to the MK[10:0] pins at row[2:0] time.
- Switch data: These locations hold the BR information read from the BR[10:0] pins at row[3:0] time.
- ADC data: These locations represent the analog voltage at VIN pin at row[3:0] time, from 0 (VIN = AGND) to 03FFH (VIN = VA33). ADC data are sampled with 10-bit precision and the result is stored on 8 bits.

12.6   GPIO

P[3:1] are controlled by the ATSAM97xx config and control/status registers (refer to prgdvkit.pdf).

P0 in normal mode is controlled by the ATSAM97xx config and control/status registers (refer to prgdvkit.pdf).

The ATSAM2553 additional GPIO control/status register controls P0 normal and alternate mode.

The GPIO register is located at address 0xF in the I/O mapping.

Data bit number	Write	Read
7	x	x
6	x	x
5	x	x
4	P0 Alt	P0 Alt
3	x	DBCLK
2	DBDATA OUT	DBDATA IN
1	DBACK	DBACK status
0	DBDATA Output Enable	DBCLK

PO:

	Normal Input	Normal Output	Alternate Output
SAM2553_config_Reg[0] (I/O add0)	0	1	1
SAM2553_GPIO_Reg[4] (I/O addF)	x	0	1

In alternate output mode, GPIO0 = Row4.

13. Revision History

Document Ref.	Comments	Change Request Ref
6399A	First issue.	

![ATMEL logo]

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